# Profile Control of Polysilicon Lines with an $SF_6/O_2$ Plasma Etch Process

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ABSTRACT

Typical plasma etching techniques used in integrated circuit fabrication can generate steep topographies that cannot be covered adequately by subsequent deposition steps. An $SF_6/O_2$ plasma etching process for polysilicon using controlled photoresist erosion produces tapered edge profiles compatible with step coverage requirements. The degree of taper is a function of the photoresist profile, the photoresist to polysilicon etch rate ratio, and the extent of overetch. The photoresist and the polysilicon appear to etch predominantly anisotropically with the isotropic component of the polysilicon etch rate increasing during the overetch period.

High resolution photolithographic techniques and plasma etching processes are required for the manufacture of fine line semiconductor devices. Typical anisotropic or isotropic plasma etching processes can produce vertical profiles or profiles approaching 90° at the top of the step that cannot be covered adequately by subsequent deposition steps. Examples of this problem are metal coverage of contact windows etched through silicon dioxide by an anisotropic technique or metal lines crossing conformal $SiO_2$ layers covering anisotropically etched polysilicon lines. A thermal reflow of the $SiO_2$ layer is often applied to minimize these problems but can result in undesired dopant diffusion or degradation of radiation hardness in MOS devices. By eroding the edges of the photoresist mask during a plasma etch, a coverable tapered profile can be formed on the etched feature. In this fashion, the photoresist profile can be transferred to the film being etched if the thicknesses and etch rates of the film and the photoresist are similar. Controlled photoresist erosion (1-5) and flexible diode (6) methods have been employed to obtain tapered profiles on plasma etched patterns. Reports on these techniques have generally given qualitative results.

This work describes the plasma etching of tapered polysilicon lines with an $SF_6/O_2$ process and details the relationship among the photoresist profile, photoresist etching behavior, polysilicon etching characteristics, and the final polysilicon profiles. The effects of feed gas composition, loading, and etch time on the silicon, photoresist, and silicon dioxide etch rates are discussed, and the polysilicon profile is examined as a function of the photoresist to silicon (PR/Si) etch rate ratio and the initial photoresist profile.

## Experimental

*Photolithography.*—KTI 1470J positive photoresist was dispensed onto the wafer, accelerated to the necessary spin speed, and prebaked at 90°C for 7.5 min in an infrared oven. The photoresist was exposed with Kasper Instruments Model 2001 contact aligners and dip developed using KTI 351 developer (3.5 parts water: 1 part developer) at 21°C for 60 sec. The photoresist coated wafers were baked at 90°C for 30 min in a convection oven and used either without further baking or with an additional bake at a higher temperature for a 30 min period.

*Samples.*—One hundred mm diameter wafers of <100>, 3-6 Ω-cm silicon were oxidized, patterned, and wet etched to leave one-half of the wafer bare silicon and the other half silicon dioxide. A grid pattern of KTI 1470J photoresist was applied over the wafer. These half and half wafers were used in the initial characterization of the silicon, silicon dioxide, and photoresist etch rates. Characterization of the loading effects and the etching profiles was performed using thermally oxidized 100 mm silicon wafers coated with 0.60 microns of LPCVD polysilicon. The polysilicon was phosphorus doped to give a sheet resistivity of 20 Ω/□. Some of the wafers were then coated with 0.50 μm of aluminum. Both types of wafers were coated with KTI 1470J positive photoresist and patterned with 2, 3, 4, and 5 μm lines and spaces. The aluminum coated wafers were wet etched and the photoresist removed, providing a noneroding etch mask for the polysilicon.

*Etching.*—A Plasma Therm Incorporated PK-2440, dual plasma/reactive ion etching system with a 3000W, 13.56 MHz rf power supply was used for this study. The rf power was applied to the upper electrode, and the lower wafer-containing electrode was grounded. The 24 in. diam aluminum electrodes have a separation of 2.0 in. and were temperature regulated at 30°C, lower, and 25°C, upper. Sulfur hexafluoride and oxygen were introduced using calibrated automatic mass flow controllers. The pressure was set up without wafers in the reactor and was not throttle valve controlled during the etch. The half and half samples described above were etched for 3.0 min, and the patterned polysilicon profile wafers were etched either by time or until endpoint as indicated by monitoring the 704 nm fluorine emission line. The polysilicon profile wafers were arranged symmetrically around the outside of the electrode. Eleven wafers can be accommodated per run with an etch time of 2-4 min.

*Measurements.*—Etch rates were determined using either a Tencor Alpha-Step Profilometer or by scanning electron microscopy (SEM) of transversely sectioned wafer samples. Photoresist and polysilicon profile data were obtained by SEM. The accuracy of the SEM measurements based upon comparison of the pattern pitch (4, 6, 8, and 10 μm) with the indicated magnification was within ±5% of nominal among the three SEM instruments used and the repeatability for each instrument was ±2%, relative ±σ. Samples were taken from the center of the wafer and 15-20 mm in from the edge of the wafer.

## Results and Discussion

*Etch rates.*—The Si, $SiO_2$, and photoresist etch rates and the uniformities of the etch rates across the reactor and within the wafer were optimized using the half and half wafers described above over a range of pressure, power, total flow, and percent oxygen values. The total flow, pressure, and power were fixed at 450 sccm, 150 mTorr, and 1500W, respectively. Rf discharges of $SF_6$ and $SF_6/O_2$ mixtures are particularly attractive for polysilicon etching because of the high Si etch rate and Si to $SiO_2$ selectivity displayed (7, 8). As shown in Fig. 1, the Si etch rate determined from 3.0 min runs with two half and half samples per run is reduced as the percent $O_2$ is increased. This effect has been attributed to competition between oxygen atoms and fluorine atoms for chemisorption on the silicon surface (5). The etch rate data replotted in Fig. 2 as etch rate ratios demonstrate that the Si to $SiO_2$ selectivity can be maintained above 10-1 while bringing the PR/Si etch rate ratio to approximately one to one.

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Key words: semiconductor, plasmas, etching.

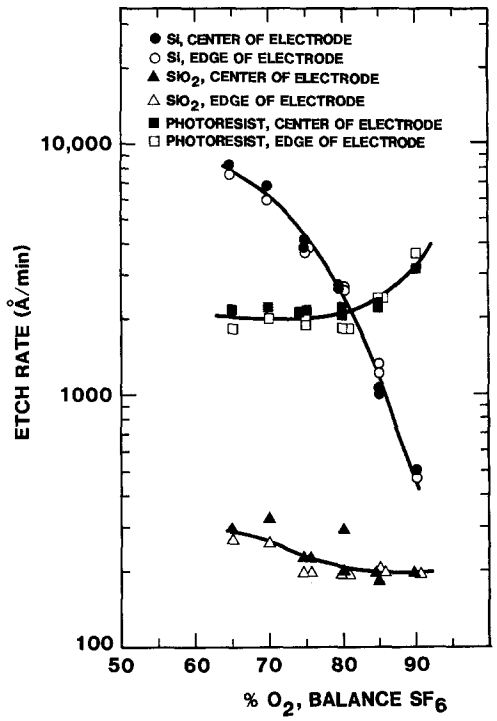


Fig. 1. The effect of percent $O_2$ in $SF_6$ on the etch rates of <100> Si, $SiO_2$, and AZ 1470J photoresist.

A typical loading effect using the patterned polysilicon wafer samples is observed for this system with the inverse of the polysilicon etch rate proportional to the number of wafers in the reactor (9). These data are plotted in Fig. 3 as the photoresist to silicon etch rate ratio *vs.* the number of wafers, since the photoresist erosion rate is relatively constant under these conditions. By adjusting the percent $O_2$ in the etchant mixture, the loading curve can be shifted to accommodate varying numbers of wafers at a given PR/Si etch rate ratio. Silicon dioxide does not exhibit a significant loading effect in this system.

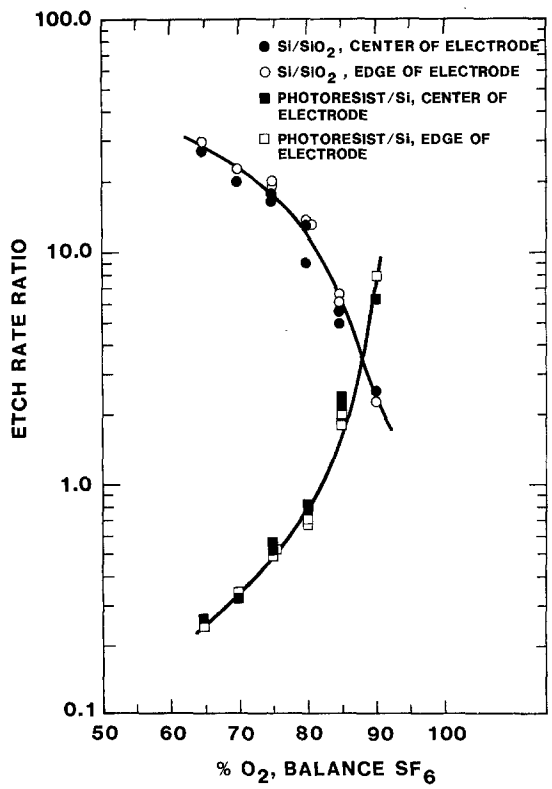


Fig. 2. The effect of percent $O_2$ in $SF_6$ on the <100> $Si/SiO_2$ and photoresist/Si etch rate ratios.

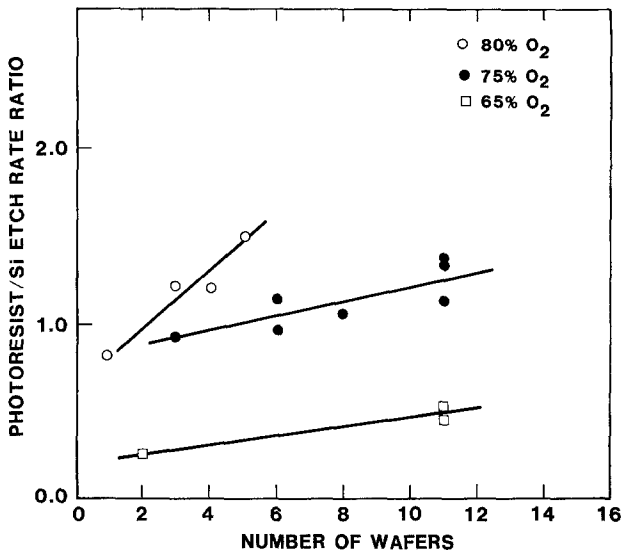


Fig. 3. The effect of loading on the photoresist/polysilicon etch rate ratio.

The PR/Si etch rate ratios derived with the patterned polysilicon sample are based on etching the wafers to completion using the 704 nm fluorine emission line to detect the endpoint. These etch ratios are, in fact, averages, since the polysilicon etch rate is proportional to the etch time. This effect is illustrated in Fig. 4 for a six wafer load and a 75% $O_2$/25% $SF_6$ mixture. Separate runs are used to obtain data for each etch time. Similar effects have been observed in barrel etching and were attributed to heating of the wafers during the etch (10). Although the electrodes are temperature controlled, the wafers may be thermally isolated since they are not in hard contact with the electrode surface. Inspection of the wafers in various stages of the etch demonstrates that the etching is nonuniform with the wafers etching radially inward on the electrode and radially inward on the wafer. This gives a lopsided bull's-eye appearance to partially etched wafers. An interesting feature of the etch rate *vs.* etch time data is that the deviation in the etch rate uniformity, wafer center to wafer edge, becomes more severe as the etch progresses.

*Photoresist profiles.*—The shape and the etching characteristics of KTI 1470J photoresist can be altered by the temperature of the postdevelopment bake. Examination of photoresist lines after a 90°C, 30 min bake reveals a steep wall profile. Photoresist lines baked at 90°C for 30 min, then at 140°C for 30 min, show a dome shape, the profile of which can be closely

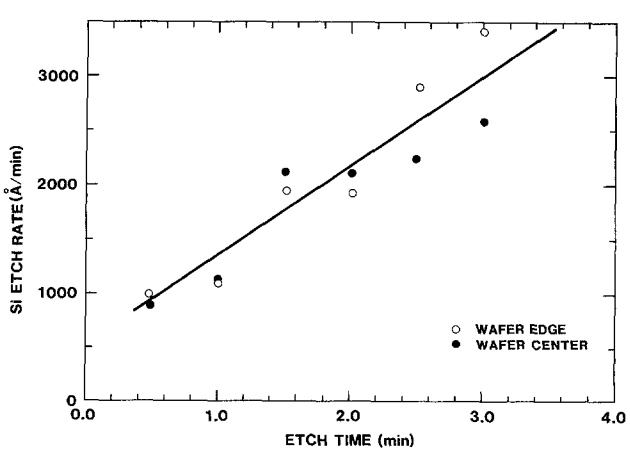


Fig. 4. The time dependence of the polysilicon etch rate

approximated by a segment of a circle. The two stage bake appears to increase the reproducibility of this process. The doming of the photoresist lines thins the edges of the line, enhancing the etching at the base. This may occur through a densification of the edges of the line by release of volatile components. While the width of the photoresist line at the base does not change upon baking at 140°C, the thickness of the line does change and is a function of the linewidth. Two, three, four, and five micron wide photoresist lines of 1.1-1.2 $\mu$m thickness after baking at 90°C will yield thicknesses of 1.0-1.1, 1.1-1.2, 1.2-1.3, and 1.3-1.4 $\mu$m, respectively, after baking at 140°C. At 165°C and above, melting of the film will occur, causing severe distortion of the pattern.

*Polysilicon profiles.*—Under the conditions employed for polysilicon etching outlined in this work, the photoresist appears to etch anisotropically. The curves in Fig. 5 illustrate the side loss expected for photoresist lines of 3, 4, and 5 $\mu$m (thicknesses 1.2, 1.3, and 1.4 $\mu$m, respectively) baked at 90°C for 30 min and 140°C for 30 min as a function of the thickness lost for isotropic etching and anisotropic etching, assuming a circular segment profile. The anisotropic etching mechanism is more consistent with the experimental data, although these data show a lot of spread. The photoresist etch rate shows little dependence upon gas composition from 65 to 80% $O_2$, wafer load in the reactor, or bake temperature, and averages 2200 ± 250 Å/min ($\pm\sigma$) on patterned polysilicon test samples. It is evident from Fig. 5 that a 5 $\mu$m photoresist line will give a greater side loss than a 3 $\mu$m photoresist line for a given thickness loss. The profiles of the etched polysilicon lines are, therefore, linewidth dependent, with the smaller lines steeper than the larger lines. This effect is illustrated in Fig. 6 for 140°C baked photoresist lines at three PR/Si etch rate ratios. The angle, $\theta$, is defined in the inset to Fig. 6. Although the polysilicon profiles observed in this study may appear slightly convex or concave, an overall angle can easily be assigned and

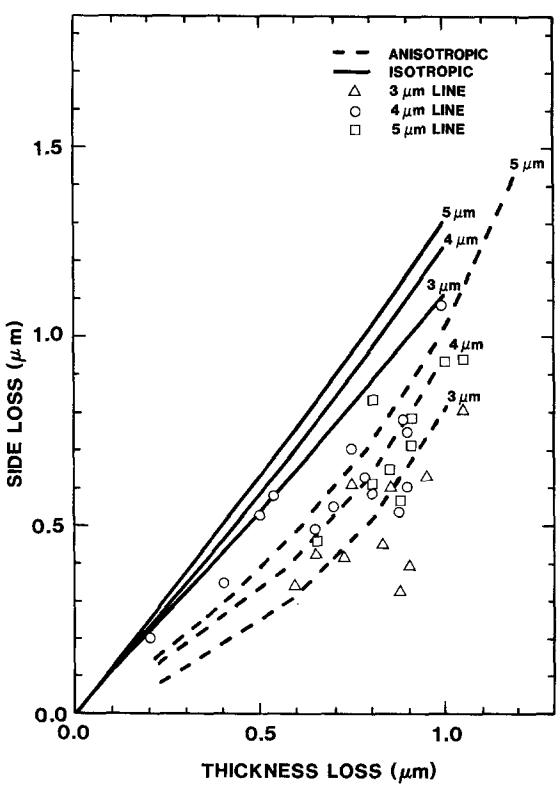


Fig. 5. The effect of thickness loss on the side loss for AZ 1470J photoresist lines baked at 90°C for 30 min and at 140°C for 30 min. The dashed lines and the solid lines illustrate the side loss expected for anisotropic and isotropic photoresist etching, respectively.

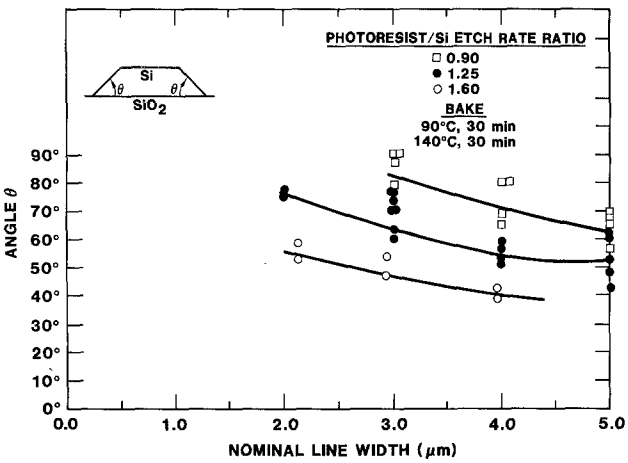


Fig. 6. The influence of the photoresist linewidth and the photoresist/polysilicon etch rate ratio on the polysilicon line taper for photoresist baked at 90°C for 30 min and 140°C for 30 min.

provides a useful first-order approximation to the line shape. When significant curvature was present, the steepest assignable angle characterized the profile. A typical polysilicon profile with the photoresist on the line is shown in Fig. 7. The angles formed are a function of the PR/Si etch rate ratio indicating that photoresist edge erosion is controlling the polysilicon line profile. In general, the more photoresist removed during the etch, the smaller the polysilicon slope angle produced. Photoresist lines baked at 90°C erode more slowly at the edge, producing steep (large $\theta$) polysilicon line profiles that are not dependent upon linewidth and PR/Si etch rate ratio. These data appear in Fig. 8.

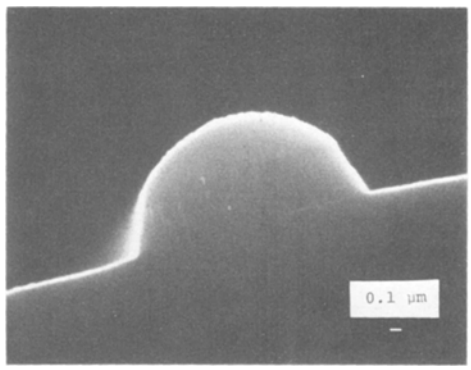


Fig. 7. SEM photograph of a 2 $\mu$m wide polysilicon line with photoresist.

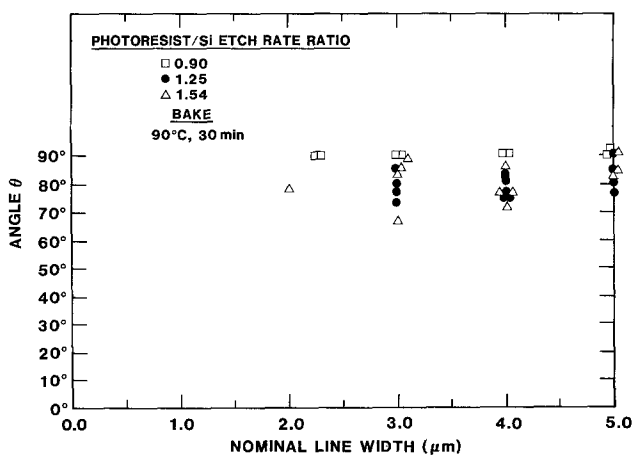


Fig. 8. The effect of the photoresist linewidth and the photoresist/polysilicon etch rate ratio on the polysilicon line taper for photoresist baked at 90°C for 30 min.

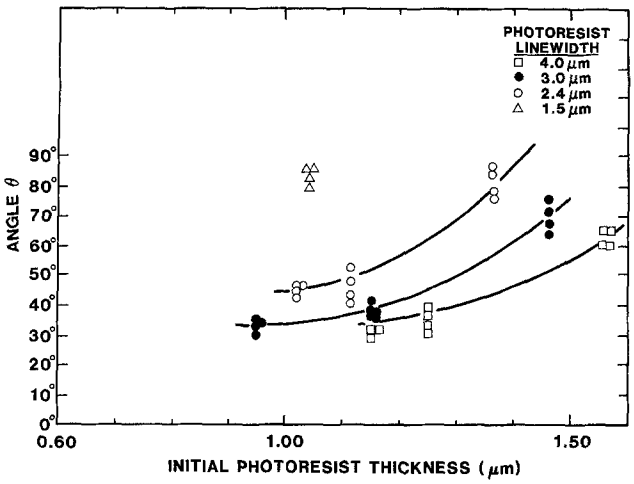


Fig. 9. The influence of initial photoresist thickness on the polysilicon line taper.

An alternative to manipulating the PR/Si etch rate ratio for obtaining sloped lines is variation of the photoresist thickness. The natural thinning of the photoresist over steps forms the practical limit for this sloping technique in device production. Figure 9 demonstrates the effect of initial photoresist thickness (140°C bake) on line slope for several linewidths at a PR/Si etch rate ratio of 1.6. The linewidth dependence discussed above is clearly evident in these data.

SEM data of lines etched with either aluminum masking or with photoresist baked at 90°C indicate a substantial anisotropic component with the vertical etch rate at least twice the lateral etch rate. The detailed dependence of the anisotropic component on the plasma parameters is currently being investigated. The profile data suggest that a change in the degree of anisotropy occurs as the polysilicon lines begin to overetch. As mentioned above, the polysilicon etch rate is nonuniform across the wafer resulting in a bull's-eye effect. The extreme outside of a wafer may receive as much as a 50% overetch during a typical run. The overetch tends to steepen the slopes and reduce the linewidths. A completely anisotropic overetch at etch rates typically observed during overetch period does not account for either the amount of linewidth loss at the base of the line, or the angles observed. However, an isotropic overetch is consistent with the linewidth loss and the steepening of the angles. Figure 10 illustrates the change in step angle and linewidth at the base of the polysilicon line as a function of the PR/Si etch rate ratio for a 4 μm wide, 1.2 μm thick photoresist line baked at 140°C. The dashed lines indicate the range of slopes and linewidths predicted using simple geometric considerations and an anisotropic photoresist and silicon etching mechanism with no overetch, with an isotropic overetch, and with an anisotropic overetch at (3000 Å/min overetch rate, beginning 1.0 min before the endpoint). While this model is consistent with the data, the exact roles of time dependent phenomena such as wafer temperature and the change in local loading during the approach of the endpoint remain undefined. Further work will be necessary to fully characterize this complex etching mechanism.

## Conclusion

The profiles of plasma etched polysilicon lines are determined by the relative rates of photoresist and polysilicon etching and the photoresist profile. The average silicon etch rate can be adjusted by varying the percent $O_2$ in $SF_6$ and the number of silicon wafers in the reactor while the photoresist and $SiO_2$ etch rates remain relatively constant. In this manner, the PR/Si etch rate ratio can be set independent of reactor loading. The photoresist line profile is a function of post-development bake temperature and assumes a semicircular profile after baking at 90°C for 30 min followed by a 140°C 30 min bake. The semicircular profile results in more rapid edge erosion of the photoresist line during the polysilicon etch than possible with photoresist lines baked only at 90°C and produces tapered polysilicon line profiles. The polysilicon and photoresist appear to etch anisotropically with the isotropic polysilicon etching component becoming dominant during the overetch period.

Production processes for 3 and 2 μm design rule technologies based on this work have been established. The 2 μm process uses a PR/Si etch rate ratio of 0.5 and yields a steep polysilicon profile, while the 3 μm process

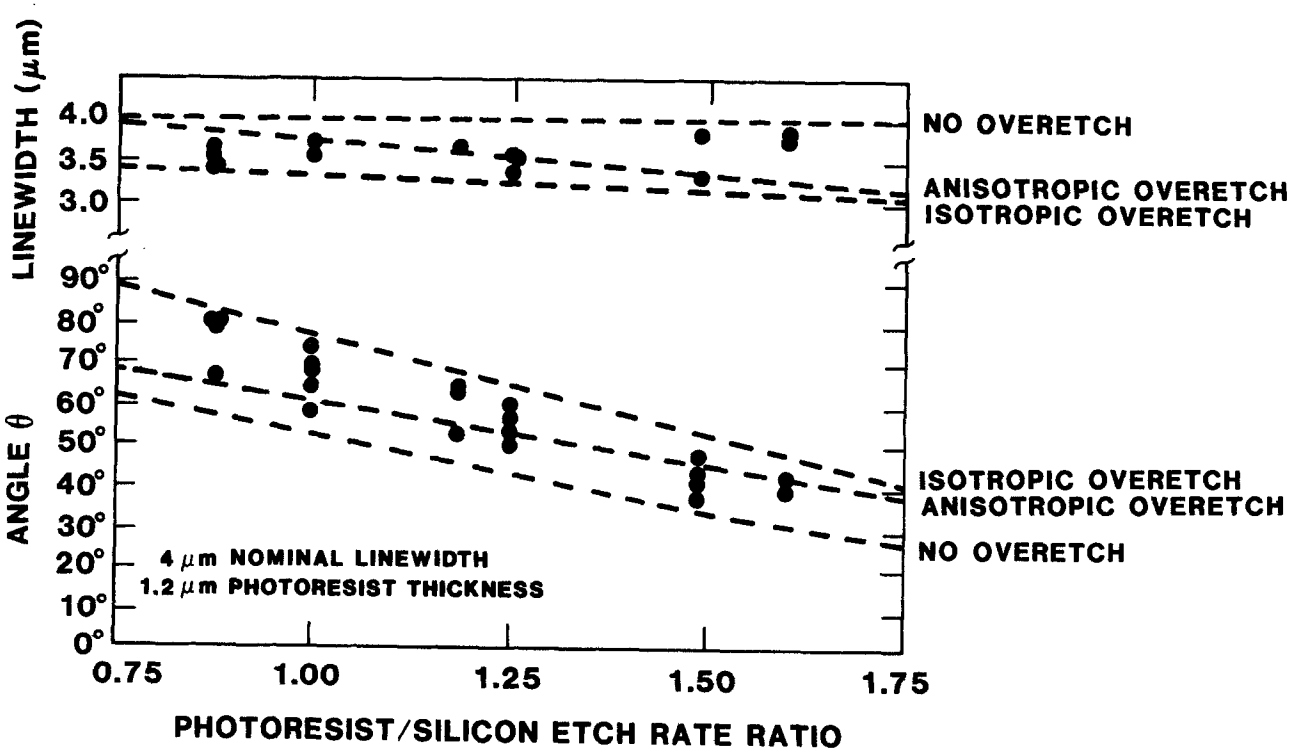


Fig. 10. The effect of the photoresist/polysilicon etch rate ratio on the polysilicon line taper and linewidth at the base

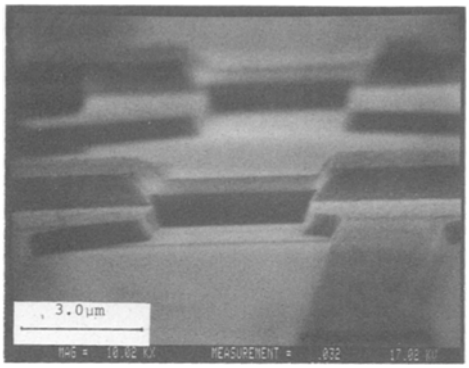


Fig. 11. An SEM photograph of an etch polysilicon pattern with the photoresist removed.

uses a PR/Si etch rate ratio of 1.2 and gives both tapered and steep polysilicon profiles. Linewidth variations of the minimum geometry polysilicon gates within the wafer and wafer to wafer are typically ±5-7%, relative $\pm\sigma$. An SEM photograph at 20° tilt of an etched polysilicon pattern in the 3 μm technology is shown in Fig. 11. The topographic and linewidth dependences of the polysilicon profile are evident in this photograph with the wide features on top of the $SiO_2$ step (middle of photograph) appearing tapered and the narrow lines in the lower, active regions (foreground of the photograph) displaying a steep profile. Step coverage of Al/Si lines crossing over underlying tapered polysilicon lines is significantly better than those crossing over underlying vertical polysilicon lines. Since a linewidth loss of 0.5-0.7 μm at the base of the polysilicon line is produced and mask biasing is necessary, this process is limited to reproducing a 4 μm pitch with 1.5 μm minimum resolution in the photoresist.

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# Growth Process of Silicon Over $SiO_2$ by CVD: Epitaxial Lateral Overgrowth Technique

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ABSTRACT

The epitaxial lateral overgrowth (ELO) process of depositing single crystal silicon over a $SiO_2$ mask is described. A CVD technique has been developed which consists of depositing silicon in openings in a $SiO_2$ mask and then growing the silicon laterally over the $SiO_2$ film. By optimizing the HCl concentration in the gas, growth temperature, and the use of a growth procedure based on a series of growth/etch steps the nucleation of polysilicon over $SiO_2$ has been eliminated and monocrystalline ELO films have been grown. Low defect density ELO films have been achieved by orientating the oxide islands along the [010] direction on (100) substrates. The growth kinetics, overgrowth morphology, and defect formation in ELO films are described as a function of the growth conditions. One can conclude that optimization of the growth process has allowed us to grow monocrystalline, low defect density ELO films with smooth mirrorlike surfaces.

A significant amount of interest has been generated in the last few years in SOI (silicon over $SiO_2$) (1). The dielectric isolation process for bipolar circuits (2) could be significantly simplified by using SOI layers if their thickness and minority carrier lifetime were sufficiently high. Also, stress enhancement of the carrier mobility observed in SOI structures (3) obtained by strip heater recrystallization of silicon films on quartz or sapphire substrates (4) could provide significant improvement in device performance. SOI structures would give an additional degree of freedom to the circuit designer in designing conventional CMOS circuits (5) and in the future could allow the achievement of three dimensional vertically integrated IC's (6).

To make state-of-the-art LSI or VLSI circuits, silicon films with a low defect density are required (7). To date graphoepitaxy (8), seeded or unseeded electron beam, laser recrystallization (1) or strip heater methods (4) have been used to obtain continuous SOI films. To improve the surface morphology of the recrystallized films, $SiO_2$ or $Si_3N_4$ caping usually has to be used to contain recrystallizing silicon during annealing. To obtain good quality films, contact with the single crystal substrate to provide a seed for solidification is required. Laser annealing is a low temperature

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