Plasma Etching of Polysilicon and Si_3N_4 in SF_6 with Some Impact on MOS Device Characteristics

W. BEINVOGL, H. R. DEPPE, R. STOKAN, AND B. HASLER

Abstract—**Accurate delineation of the circuit materials polycrystalline silicon ("poly"), and silicon nitride are important requirements of most SFC process sequences. We have investigated the use of SF_6 as an active species in the parallel-plate plasma etching of these materials. For the etching of poly there is good selectivity (better the 50:1) with respect to the etch rates of SiO_2 and positive photoresist. This process has been used in the fabrication of MOS transistor with 3-μm poly-gate lengths and threshold voltages vary by less than 0.05 V both across a wafer and from wafer to wafer. Etching of nitride is less selective and less isotropic than that of poly.**

I. Introduction

MICROFABRICATION techniques for integrated circuits are rapidly progressing towards higher packing density. With continuously decreasing lateral dimensions, the fidelity in pattern transfer becomes more and more important. Dry-etching techniques capable of providing better dimensional control than conventional wet processes, therefore, have attracted much attention in research during the last years and have partly been introduced into fabrication lines.

Anisotropy of etching which enables this accurate pattern transfer is only one of the important characteristics of a dry-etch process. Other features such as selectivity, integrity of mask material, and uniformity on the wafer, between wafers, and between lots can be of equal importance in practical application. For example, in case of etching polysilicon to define the gate areas of polysilicon-gate MOSFET's, the well-known threshold-voltage dependence on channel length ("short-channel effects," [1], [2]) makes uniformity of etching extremely important. The most direct criteria to judge the quality of an etching procedure are apparently the electrical characteristics of the devices.

Several procedures for dry etching of polysilicon have been reported on both in the plasma-etch (PE) mode (wafers on grounded electrode, pressure usually >30 Pa) and in the reactive-ion-etch (RIE, RSE) mode (wafers on RF-driven electrode, pressure typically a few pascals). For PE, various mixtures of fluorine- and chlorine-containing gases have been used [3], [4] as well as CF_4 [5] and SF_6 [6]. Etching with SF_6 has also been carried out in a single-wafer reactor [7]. Concerning the RIE mode, mainly procedures using CF_4 [8] and SF_6 [9]-[12] have been described in the literature.

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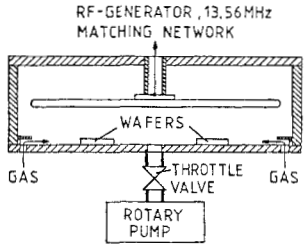

Fig. 1. Schematic diagram of the radial-flow batch-type reactor.

Less information has been published on silicon nitride etching. CHF_3 can be used to etch Si_3N_4 anisotropically [13], [14]. Also $CF_4 + O_2$ is reported for nitride etching [15] in a parallel-plate reactor. In this paper, we report on results in polysilicon and Si_3N_4 etching in a parallel-plate batch-type reactor using sulphurhexafluoride as the etch gas. For both cases, electrical characteristics of MOS devices are presented to examine the quality of etching procedures.

II. Experimental

The etching processes have been developed in a commercially available batch-type reactor which is schematically illustrated in Fig. 1. The gas flow is radial with the gas inlet at the circumference of the base plate. Both electrodes are made of aluminum. The electrode spacing is adjustable and the parallelism of the electrodes has to be controlled exactly. Process parameters such as pressure, flow rates, and RF power are automatically controlled. Wafers are placed on the base plate (grounded) the temperature of which is kept constant during etching. The maximum load capacity of the reactor is twenty 100-mm wafers.

III. Polysilicon

A. Etching

The polysilicon layers which were investigated in this work were deposited using standard LP CVD techniques. Thickness is around 0.5 μm. Mostly, layers heavily doped with phosphorus were used but the results described below also essentially apply to undoped layers. Lithography was done on a 10:1 step-and-repeat system so that linewidth variations caused by lithography were minimized (compared to full wafer projection printing). Throughout this work, AZ1350H photoresist was used as etch mask. Postbake temperature of the resist has been kept low enough to avoid any noticeable change of the resist profile due to thermal flow.

In Fig. 2, etch rates of polysilicon, thermal SiO_2, and the photoresist as well as the corresponding selectivities are plotted

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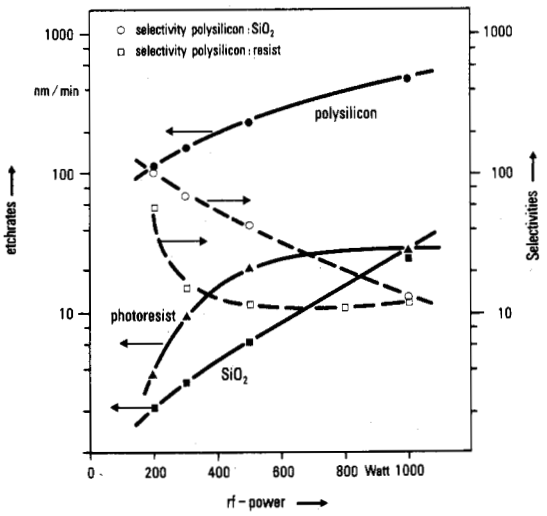

Fig. 2. Etch rates and selectivities on a logarithmic scale as a function of RF power. SF_6 is diluted with He at a ratio of 1:2. All etch rates are for a single 100-mm wafer.

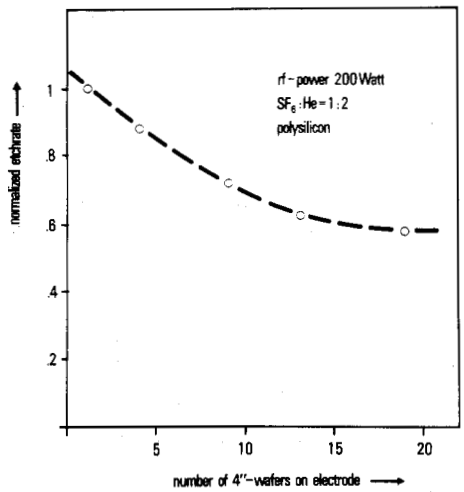

Fig. 3. Loading effect for polysilicon etching. Etch rates are normalized to the value for a single 100-mm wafer.

as a function of RF power. The polysilicon etch rate is between 100 and 500 nm/min in the power range depicted in Fig. 2. It increases approximately linearly with the RF power. This finding differs from results reported about RIE with SF_6 where the etch rate of polysilicon only weakly depends on RF power [10]. Note also in Fig. 2 the rather sharp increase in selectivity to SiO_2 and resist in the low-power regime. At 200 W, polysilicon etches 100 times faster than SiO_2. Selectivity polysilicon: resist (as defined as the ratio of etch rates in vertical direction) is also larger than 50:1.

Polysilicon etching in SF_6 exhibits a loading effect, as can be seen in Fig. 3. There the etch-rate dependence on reactor load is shown under constant SF_6 dilution and gas-flow condition. This undesirable loading effect is typical for fluorine-based polysilicon etching. The etch rate for the fully loaded reactor (20 wafers) is about 40 percent lower than for a single wafer. The loading effect has been modeled in [16]. It predicts a dependence of etch rate a on wafer number N of the form $a(N) = C_1 \times (1 + C_2 \times N)^{-1}$ where C_1 and C_2 are constants for fixed-process conditions. Fig. 3 approximately follows this relation. The magnitude of the loading effect, i.e., of constant C_2 (which contains the lifetime of reactive species and the kinetic rate constant for the etching reaction) is in our case relatively small compared to $CF_4 + O_2$ [16]. There, an etch-rate variation by a factor of 4 between 1 and 10 wafers loaded into the reactor has been reported on.

SF_6 apparently is an etch gas which is able to release a large amount of fluorine. We usually diluted SF_6 with He because in this way RF impedance matching and plasma stability were easier to achieve. Even when a dilution $\gtrsim 10:1$ ($He:SF_6$) was used, polysilicon was still etching with a reasonable rate.

When etching polysilicon with fluorine-containing gases, very often nonuniform etching over a wafer is found in such a form that the etch front proceeds from the edge to the center of the wafer. This behavior which is related to the depletion of active species leads to thinning of the underlying oxide as well as to an undercut varying over the wafer and, as already mentioned, this is a very undesirable effect. This kind of nonuniformity was found to be much weaker in SF_6 compared to CF_4 under similar conditions. However, this advantage of SF_6 holds only within a certain parameter range and in the PE mode. Working in the RIE mode, the etch rates were generally higher under comparable conditions but we were not able to achieve a uniformity as good as that in the PE mode.

Typical etch profiles obtained for a 0.5-μm-thick polysilicon layer are shown on the right-hand side of Fig. 4(a). For zero overetch time, rather long polysilicon tails are found along the resist edge whereas the undercut, when measured at the top of the layer, is 0.15 to 0.2 μm. This indicates that etching is not purely isotropic. In that case, the undercut would have to be equal to film thickness. When overetch time increases (middle and lower part of Fig. 4(a)), the tail disappears and the polysilicon sidewall becomes steeper. For 60-s overetch time, the undercut amounts to about 0.4 μm. From these facts, it can be concluded that the procedure is well suited for single-layer polysilicon etching as long as a loss of about 0.2 μm in feature size can be compensated on the mask level.

A certain and well-controlled amount of undercut is not only tolerable but necessary for some applications. An example, given in Fig. 5, shows part of an MOS integrated circuit with two polysilicon layers. The second poly layer has been etched strictly anisotropically (RIE) according to a procedure described in [12]. A ribbon of the second polysilicon level can clearly be seen along the polysilicon edge of the first layer connecting adjacent areas of the second level due to strictly anisotropic etching. A similar structure is shown on the left-hand side of Fig. 4(a). In this case, (PE) polysilicon-2 residues are thinned in the overetch period due to the lateral attack. After 1-min overetch, only some isolated grains of the polysilicon-2 layer remain. On the other hand, the thickness of the underlying gate oxide only decreases by about 2 nm during overetch time due to the very high selectivity. The topography shown in the SEM's on the left-hand side of Fig. 4(a) is schematically illustrated in Fig. 4(b).

Etching of a polysilicon layer can be completed in one step without changing process conditions since dimensional control is acceptable and selectivity to SiO_2 is very high. Because of the extremely small resist etch rate, no measureable change of resist linewidth during etching occurs. This holds even for

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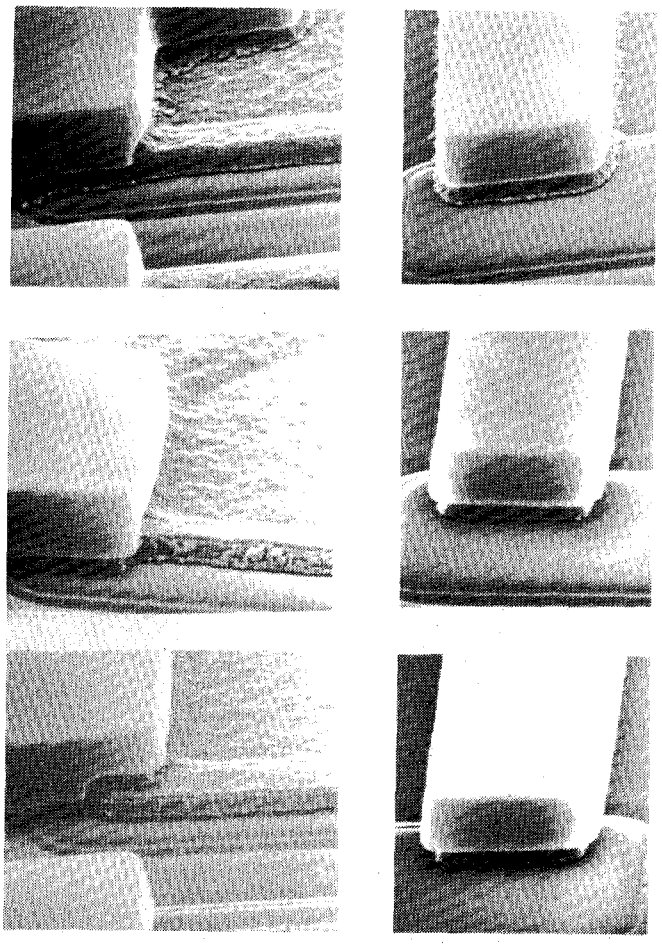
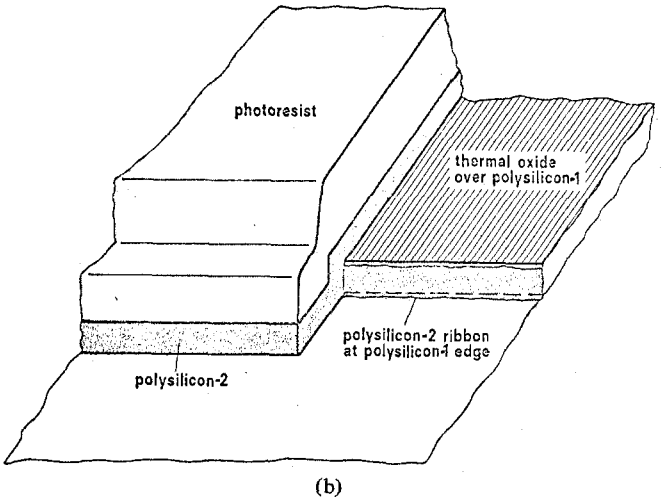


(a)



(b)

Fig. 4. (a) Right side: SEM micrographs of polysilicon lines (layer thickness 0.5 μm) for three different overetch times. Left side: Polysilicon-2 ribbon at polysilicon-1 edge as a function of overetch time t (top t = 0 s, middle t = 20 s, bottom t = 60 s). The topography is explained in (b). (b) Schematic illustration of the two polysilicon layers with the polysilicon-2 ribbon along the polysilicon-1 edge. Resist over polysilicon-2 is still in place.

rather flat (40°-50°) resist sidewall angles. The very low power density during etching positively affects uptime of the machine and minimizes possible radiation damage on the wafers as well as energy consumption. For device applications, the question

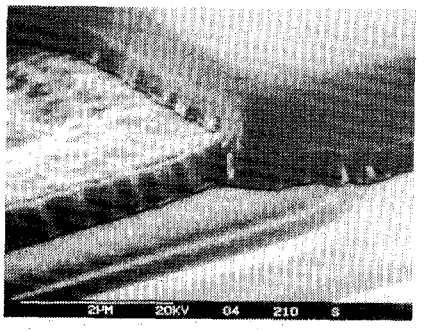


Fig. 5. SEM micrograph showing a part of a highly integrated MOS device where the polysilicon-2 layer has been strictly anisotropically etched (RIE) using SF_6. Note the ribbon at the polysilicon-1 edge.

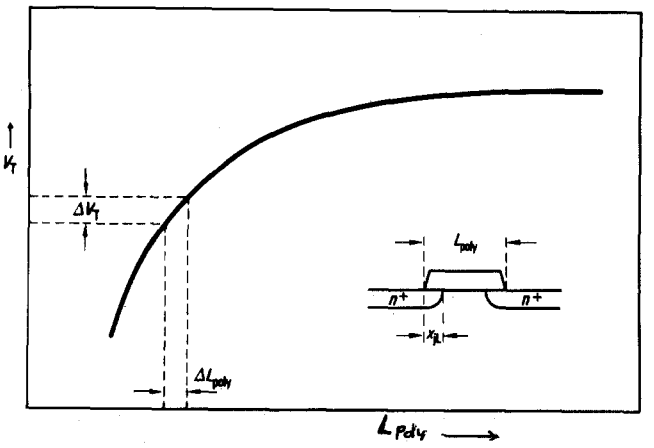


Fig. 6. Dependence of threshold voltage V_T on channel length L_{Poly} of MOSFET's (schematically). The quantitative "short-channel effect" is strongly influenced by specific fabrication steps.

of possible contamination of the wafer surface due to sulphur-containing residues is of great importance. Several wafers have been analyzed after etching with standard Auger techniques. No sulphur has been found. The detection limit of the Auger system was 0.1 at %.

According to the results presented so far, the procedure seems to be suitable for application in IC fabrication.

B. Impact on MOS Device Characteristics

One of the key features in VLSI circuit fabrication is accurate control of the polysilicon linewidth because it defines the channel length of a MOSFET in a standard n-channel polysilicon-gate process to which we refer in the following examples. In VLSI circuits, the threshold voltage V_T of MOSFET's not only depends on standard parameters (gate-oxide thickness, channel doping concentration) but also very sensitively depends on the channel length. This short-channel effect (SCE) has been described in [1], [2]. The insert in Fig. 6 schematically illustrates the relationship between the polysilicon linewidth L_{Poly} and the effective channel length $L_{eff} = L_{Poly} - 2x_{jL}$. x_{jL} means the lateral diffusion of the heavily doped source-drain regions and is dependent on the detailed fabrication steps. Keeping x_{jL} constant (in our case typically 0.4 μm) variations in L_{eff} are mainly due to linewidth variations of L_{Poly}. Fig. 6 qualitatively illustrates the SCE: V_T decreases as a function of L_{Poly}. The quantitative behavior of V_T in the region of small values of L_{Poly} (typically <5 μm) strongly de-

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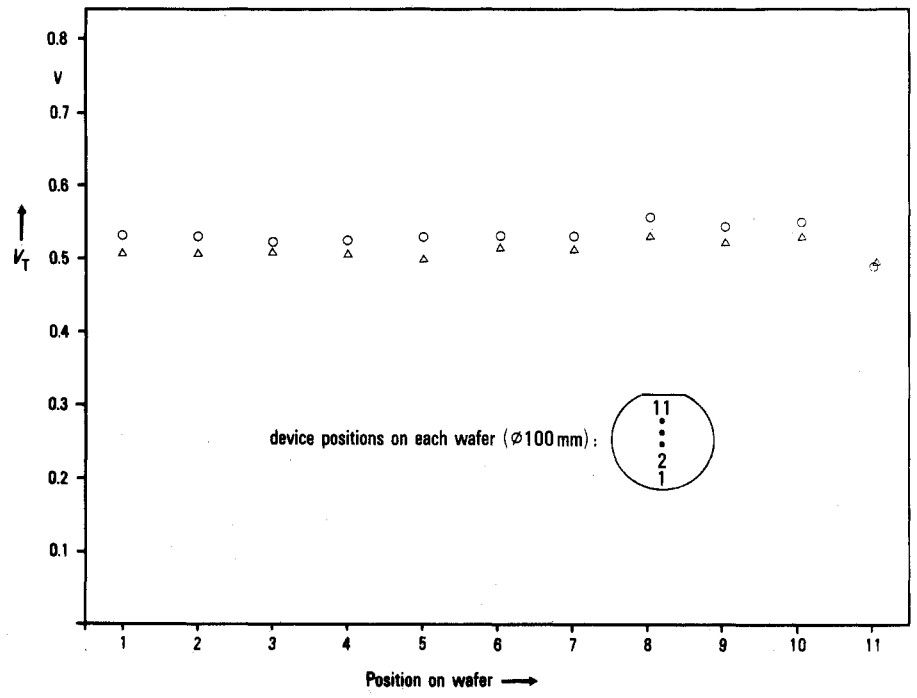

Fig. 7. V_T variation of a test MOS transistor (W/L = 30/3) measured on 2 wafers (△—no. 1, ○—no. 27) randomly selected from a lot. The insert shows the measurement positions on the wafer.

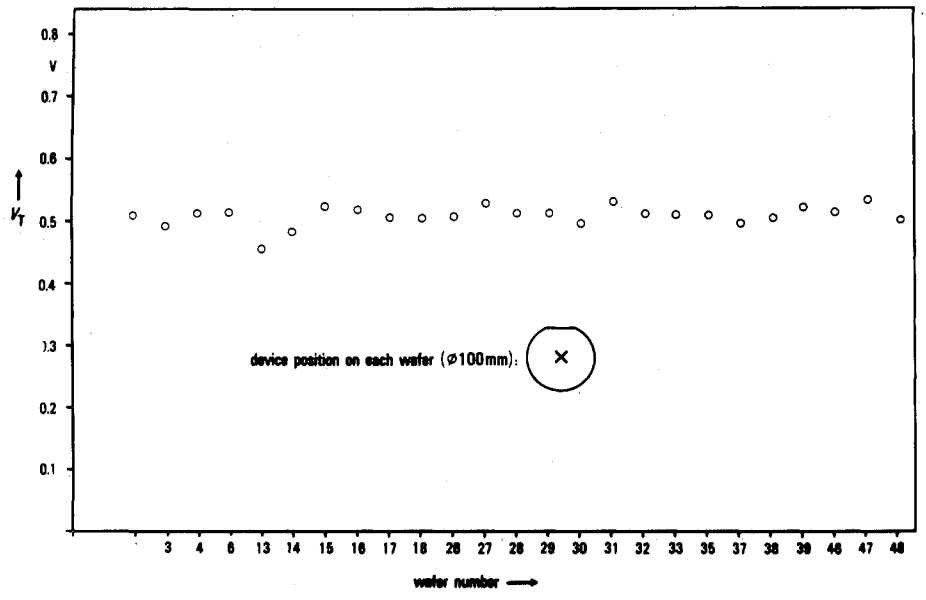

Fig. 8. V_T variation of the same test device as in Fig. 6 (W/L = 30/3) over 25 wafers selected at random from one lot. The device position on the wafers is shown in the insert.

pends on fabrication parameters and measurement conditions. The MOS test devices used for the following examples have L_{Poly} around 3 μm and, therefore, we are in the short-channel region where ΔV_T is mainly determined by ΔL_{Poly}.

Fig. 7 shows typical V_T distributions of two 100-mm wafers. V_T variations smaller than ±30 mV over one wafer have been achieved. It should be noted that under our measurement conditions (drain-to-source voltage +5 V, substrate voltage −2.5 V) the short-channel effect becomes more pronounced. Using the quantitative dependence V_T (L_{Poly}) for our case, ΔL_{Poly} values of ±0.25 μm are obtained corresponding to ΔV_T = ±30 mV. These variations include all other process influences such as those of lithography, gate-oxide thickness, channel doping, etc. The device positions on the wafer, shown in Fig. 7, are parallel to the direction of gas flow in the reactor chamber. This direction was found to be more critical with respect to etching nonuniformity than perpendicular to the device positions shown in the figure. Therefore, Fig. 7 shows maximum V_T variations over the whole wafer.

Apart from this rather good uniformity over a single wafer, the variation from wafer to wafer is of equal importance in a batch process which we are using. Fig. 8 shows V_T values of

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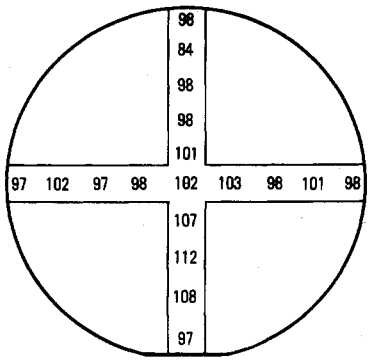

Fig. 9. Thickness of gate oxide (in angstroms) measured on 18 chips of a 3-in wafer after polysilicon etching. Oxide thickness has been determined prior to polysilicon deposition (110 Å in the center of the wafer).

25 wafers taken at random from one lot. The device position is at the center of each wafer. V_T values vary within the range of ±40 mV which is approximately of the same magnitude as the variations obtained on a single wafer. This demonstrates that very small polysilicon linewidth variations can be achieved in batch-type etching using appropriate process conditions.

Beside a high fidelity of pattern transfer in the fabrication of VLSI circuits, selectivity to underlying gate oxide becomes more and more important since oxide thickness continuously decreases with increasing packing density, e.g., in case of 256K DRAM, gate oxides are in the range of 20 to 30 nm. As shown in Fig. 2, a selectivity polysilicon: SiO_2 of 100:1 can be realized. This leads to a very small gate oxide thinning, as demonstrated in Fig. 9. The gate oxide on this wafer has been measured to be 11 nm in the center of the wafer before polysilicon deposition. The numbers in Fig. 9 represent the gate-oxide thickness after polysilicon etching on 18 chips of the same wafer. Almost all of the oxide layer remains after etching. As a consequence, even in the case of very thin gate oxides, one can avoid attacking of the silicon substrate which can lead to degradation of electrical characteristics due to contamination and damaged layers [17].

IV. Silicon Nitride

A. Etching

Silicon nitride layers investigated in this work have been deposited with LP CVD. Mainly layers with a thickness around a 0.1 μm on top of a thin thermal oxide (~50 nm) have been etched to define the active areas before local oxidation. As to resist and lithography, the same as for polysilicon applies.

Generally, both the etch rate for Si_3N_4 and selectivity to SiO_2 are much lower than for polysilicon. Fig. 10 shows the dependence of etch rates on SF_6 gas flow. The Si_3N_4 etch rate is between 40 and 20 nm/min. With a higher SF_6 flow rate, a selectivity of 6:1 to thermal SiO_2 is reached. The loading effect is generally considerably smaller than for polysilicon. It amounts to an increase of 10 percent in etch time (flow rate of SF_6 = 25 sccm, 500 W) when the reactor is fully loaded compared to a single wafer. The less pronounced loading effect is consistent with the decreased etch rate in case of Si_3N_4. C_2 in the formula mentioned before contains the kinetic rate constant of the surface reaction between the reactant and the material to be etched. Therefore, a lower etch rate is expected to diminish the loading effect. The decrease of the etch rate with an increase in SF_6 flow rate is difficult to understand. A similar behavior has been found in case of Si_3N_4 etching in a barrel-type reactor [18]. There, it has been attributed to a flow-limited lifetime of reactive species. This seems to be unlikely in our case where the residence time is several seconds.

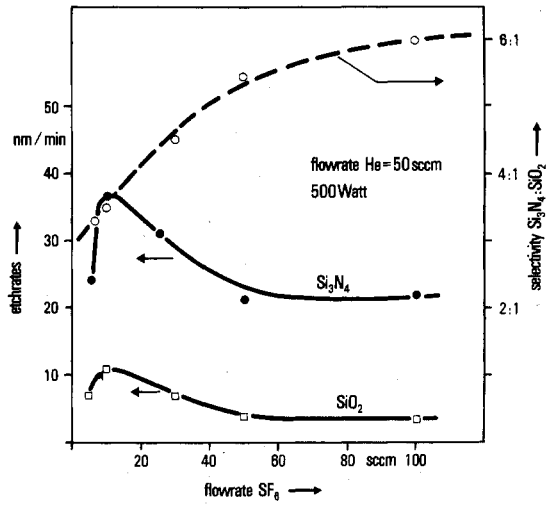

Fig. 10. Etch rates for Si_3N_4 and thermal SiO_2 and the corresponding selectivity as a function of SF_6 gas flow.

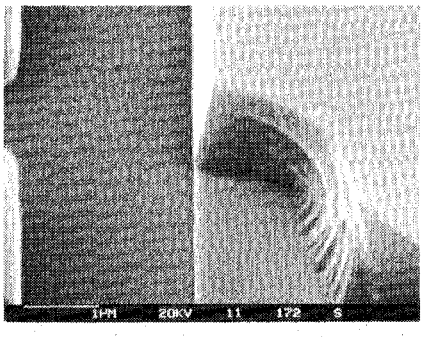

Fig. 11. SEM micrograph showing a part of a nitride line on top of a thin SiO_2 layer. A part of the resist has been removed to demonstrate the anisotropy of pattern transfer.

Si_3N_4 etching is essentially anisotropic. Fig. 11 shows part of an Si_3N_4 line where the resist has partly been removed. No loss in linewidth underneath the resist can be seen. Also when much thicker layers (around 1 μm) have been etched, the profile was essentially anisotropic.

B. Electrical Results

In order to test the accuracy of pattern delineation for Si_3N_4 capacitance measurements of memory-cell test arrays have been performed. Keeping gate-oxide thickness constant, the capacitance is determined by the active area which is defined by nitride etching before local oxidation. Thus different values of nitride undercut cause changes in capacitance. This is demonstrated in Fig. 12. The figure shows the measured capacitance which is normalized to the theoretical value for

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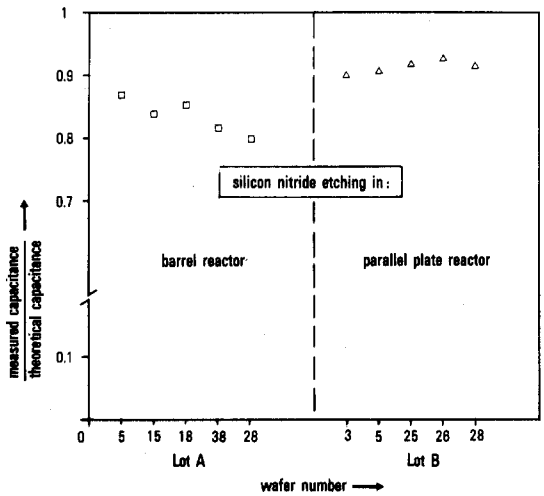

Fig. 12. Normalized storage capacitance of a memory-cell test array in standard MOS technology and its dependence on nitride etching process in different reactor types. Wafers have been taken at random from two different lots.

ten 100-mm wafers. For those of lot *A*, nitride has been etched in a barrel reactor in $CF_4 + O_2$ whereas those of lot *B* have been delineated in the parallel-plate reactor with SF_6. The wafers etched in the parallel-plate reactor clearly exhibit a higher absolute value of the capacitance as well as less variations from wafer to wafer. This is caused by the anisotropy of etching in the parallel-plate reactor in contrast to the isotropic etch characteristics in a barrel-type reactor with its tendency to nonuniform undercut especially in the case of increasing wafer diameter.

V. Conclusions

We have discussed a batch-type plasma-etching process for polysilicon with SF_6. Etching was found to be mixed, both isotropic and anisotropic. The process is suitable for polysilicon etching of VLSI circuits especially with respect to selectivity and uniformity. These features have been examined in detail with electrical measurements on test devices. SF_6 has also been applied to nitride etching on top of SiO_2. Profiles are anisotropic in this case. Capacitance measurements on wafers etched in the parallel-plate reactor show a higher fidelity in pattern transfer as well as better uniformity than on wafers etched in a barrel-type reactor.

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