Isotropic Etching With Xenon Difluoride

XACTIX, Inc
Overview

• Corporate Overview
• Xenon Difluoride Etch Process
• MEMS Application Examples
• Other Application Examples
• XACTIX Equipment
XACTIX Overview

– The source for xenon difluoride etching technology
– Ten years working with premier commercial customers and MEMS R&D programs.
– Over 100 Machines installed or in Progress
– US, Japan, Taiwan, Korea, China, Europe, Canada, Malaysia
– Full time process and equipment R&D effort leading to a growing IP position.
– Sales & marketing and development agreements with STS
Location

Pittsburgh Pennsylvania

Washington D.C. - 4hrs by car
New York City - 6hrs by car
Philadelphia - 5 hrs by car
Boston, Chicago - 1.5 hrs by Airplane
San Francisco - 4.5 hrs by Airplane
## Customers By Type

<table>
<thead>
<tr>
<th>Type</th>
<th>Sales</th>
</tr>
</thead>
<tbody>
<tr>
<td>Public Companies</td>
<td>35%</td>
</tr>
<tr>
<td>University</td>
<td>35%</td>
</tr>
<tr>
<td>Private Companies</td>
<td>15%</td>
</tr>
<tr>
<td>Govt. Lab</td>
<td>15%</td>
</tr>
</tbody>
</table>
Selected Customers

Commercial
- Analog Devices
- Lucent
- IBM
- Qualcomm
- Seagate
- Corning
- Northrop Grumman
- Hitachi
- Japanese Consumer Companies

Universities and Labs
- US Army Laboratory
- NASA Goddard Space Flight Center
- National Institute of Standards
- Stanford
- Cornell
- Carnegie Mellon University
- University of Michigan
- Penn State University
- ITRI
- Ritsumeikan University
- University of Twente
• Together STS and XACTIX have over 15 years of experience with XeF$_2$
• STS distributes XACTIX products in Europe.
• STS and XACTIX jointly market XeF$_2$
  – Xetch X3, Xetch e1, Module for STS platform.
  – Joint Market Marketing Agreement
• STS and XACTIX cooperate on new products including new module for STS platform.
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Xenon Difluoride

*Isotropic Silicon Etch For MEMS Release*

- Highly Selective MEMS Release
- No Stiction Problems
- Long Undercuts
- Release Using Nano-scale Holes and Release Layers
Etching Process

- $2\text{XeF}_2 + \text{Si} \rightarrow 2\text{Xe} + \text{SiF}_4$
- Selectively etches silicon, molybdenum and germanium.
- Isotropic etching
- Dry, vacuum based process (NO plasma or other activation needed)
- $\text{XeF}_2$ sublimates from solid crystals to form the vapor-phase etchant
Bulk Silicon Surface Micromachining

Pattern Device Layers

Deposit Device Layers

Si Substrate

Isotropic Si Etch to Undercut Device
Surface Micromachining

- Define Etch Hole
- Deposit Sacrificial Layer
- Deposit Etch Stop
- Deposit Device Layers
- Deposit and Patterned Sacrificial Layer
- Substrate
Why XeF$_2$?
Improved Yield

- Minimize damage to other materials on wafer.
- Eliminate damage caused when removing protective coatings.
- Eliminate loss due to stiction caused by wet processes.
- Eliminate damage to released parts during dicing by releasing after dicing on the dicing tape.
- Eliminate damage to released parts during packaging by releasing in the package.
Why XeF$_2$?

Improved Products

• Use new, better materials
• Combine CMOS and MEMS devices on the same die.
• Shrink the size or thickness of the device to either improve performance or make room for more capabilities.
• Shrink the size of etch holes or lower the number of etch holes to minimize their effect on the performance of the device
Why XeF$_2$?
Improved Process

- Simplify the process to eliminate mask steps and other process steps.
- Eliminate wet chemical materials handling and waste disposal.
- Minimize risk during design since XeF2 is unlikely to damage materials or interact with other process steps.
Why XeF$_2$?
Expanded Research Capabilities

- Use new materials and new combinations of materials for MEMS structures.
- Shrink etch holes to unprecedented sizes.
- Shrink device geometries to unprecedented sizes.
- Shrink release layers to unprecedented thinness.
- Minimize risk and accelerate success.
As Late As Possible Release

• Once MEMS can move they can break

• Release after Capping
  – Avoid physical damage from capping process.
  – Go from release to hermetic seal under vacuum.

• Release at Packaging Fab
  – Avoid physical damage during transit
  – Avoid corrosion or stiction caused by moisture exposure after release.

• Release After Dicing
  – Avoid physical damage from vibration or heat and washing

• Release After Package Insertion and Wire Bonding
  – Avoid physical damage from vibration
  – Avoid exposure to packaging chemicals.
Etch Rates: Loading

- Typical Surface Micromachining Application with Si on 6” wafers: 2 to 3 um/min
- Small Chips: up to 10 um/min
- Fully exposed 6” wafer: 0.2 um/min
## Reactive Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Selectivity to Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1:1</td>
</tr>
<tr>
<td>Mo</td>
<td>2:1</td>
</tr>
<tr>
<td>Ge</td>
<td>Same or Faster than Si</td>
</tr>
<tr>
<td>SiGe</td>
<td>Same or Faster than Si</td>
</tr>
</tbody>
</table>
Conditionally Reactive Materials

• Ti, TiN, Ta, TaN, W, TiW
  – Etch rate depends on temperature.
  – Etch rates from 0 to 300 Å/min
Low Attack Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Typical Selectivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal SiO$_2$</td>
<td>1000:1</td>
</tr>
<tr>
<td>Low Temperature SiO$_2$</td>
<td>1000:1</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
<td>&gt;1000:1</td>
</tr>
<tr>
<td>Gold</td>
<td>Low Amount of Attack Under Certain Conditions</td>
</tr>
<tr>
<td>Copper</td>
<td></td>
</tr>
<tr>
<td>SiC</td>
<td></td>
</tr>
</tbody>
</table>
## Non Reactive Materials

<table>
<thead>
<tr>
<th>Metals</th>
<th>Compounds</th>
<th>Polymers and Organics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>PZT</td>
<td>Photo Resists</td>
</tr>
<tr>
<td>Ni</td>
<td>MgO</td>
<td>PDMS</td>
</tr>
<tr>
<td>Cr</td>
<td>ZnO</td>
<td>C$_4$F$_8$</td>
</tr>
<tr>
<td>Pt</td>
<td>AlN</td>
<td>Silica Glass</td>
</tr>
<tr>
<td>Ga</td>
<td>GaAs</td>
<td>PVC (Dicing Tape)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PEN</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PET</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ETFE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Acrylic</td>
</tr>
</tbody>
</table>
Two Types of Processes

- **Pulsed Flow**
  - Higher efficiency
  - Accurate mixing of XeF2 with other gasses
- **Continuous Flow**
  - Easier to achieve high uniformity
  - More obvious control of the etch depth
  - Easier end point detection
Continuous Flow

Pressure Controller Maintains Constant Pressure in Process Chamber

MFC Maintains a Constant Flow of XeF₂
Pulsed Flow

Fill Expansion Chamber To Specified Pressure
Close Valve
Let XeF₂ Flow Into Process Chamber
Wait For Etch Time
Pump Down
Repeat
Pulsed Flow Variations

• Mixing XeF$_2$ with Nitrogen
  – XeF$_2$ added to expansion chamber then Nitrogen
  – Improves selectivity to silicon nitride
  – Large amount of nitrogen can help achieve very slow etch rates.

• Rapid Pulse
  – User can raise the pump down pressure in the pulsed cycle which reduces process overhead.
  – Increases throughput when etching larger exposed areas.

• Pulsed Flow with Delays
  – User defines a wait time between etch pulses.
  – Primarily used to allow the sample to cool down between pulses to protect temperature sensitive materials.
New Processes

- **High Conductance Mode** *(Patent Pending)*
  - Alternates etching pulse with nitrogen pulse.
  - Reduces wafer temperature
  - Dilutes effluents
  - Increased selectivity for a number of materials, (eg. silicon nitride, TiN)

- **Continuous Mixed Gas Flow** *(Patent Pending)*
  - Allows mixing XeF<sub>2</sub> and nitrogen in a continuous flow of gas.
  - MFC and pressure controller used to control gas flow rate and process chamber pressure
  - System alternates filling the two expansion chambers to provide a regular supply of accurately mixed gasses.
  - Increased selectivity.
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Application Areas

Sample of Applications
• RF Switches
• Projection Displays
• Reflective Displays
• Optical Attenuators
• Airborne Virus Detectors
• Chemical Sensors
• Pumps
• Oscillators
• IR Sensors
• Disk Drives
• Heaters/Micro Hot Plates

Sample Structures
• Switches
• Cantilevers
• Bridges
• Mirrors
• Membranes
• Channels
• Thermal Isolation Cavities
Wide Variety of Substrates

- Silicon Wafers
- Glass
- Diced Wafers on Dicing Frames
- Diced Chips
- Chips After Package Insertion and Wire Bonding
- Non Standard Parts
Poly-Silicon Micromachining

- High selectivity, excellent reach, fast etch times make XeF$_2$ an ideal solution for surface micromachining.
- Example of Common Commercial Application: Undercut = 30um to 100um, etch rate $\sim= 3$um/min

Etch Hole $\sim 1$um$^2$  Device: Material Sandwich

Sacrificial Silicon: $\sim 400$nm Thick  Oxide Etch Stop: $\sim 200$nm thick
Al Cantilivers

- Prof. Chad O’Neal
  Louisiana Tech.
- Released using XeF$_2$. 
Al Cantilivers

- Prof. Chad O’Neal
  Louisiana Tech.
- Released using XeF$_2$. 
10 GHz AlN NEMS Resonators

- Prof. Gianluca Piazza, University of Pennsylvania
- AlN resonator released using XeF$_2$.
- Resonator is only 205nm thick.
Aultra Thin AIN NEMS Actuator

- Beam formed by 2 layers of 100 nm thick AIN
- Prof. Gianluca Piazza, University of Pennsylvania
- AIN actuator released using XeF$_2$.
- Beam is only 100nm thick.
ADI Optical iMEMS Mirror

- Analog Devices
- Silicon Micro-Mirror
- Used XeF2 to overcome selectivity problems with long etches.
- Protected silicon device with thin oxide layer during release.

T.J. Brosnihan, et al., Optical iMEMS – A Fabrication Process for MEMS Opticla Switches with Integrated On-Chip Electronics, Transducers03
Diffractive MEMS Optical Attenuator

- LIGHTCONNECT
- Released using XeF$_2$ because of selectivity to silicon nitride and aluminum.

http://www.lightconnect.com/technology/tech.shtml
iMod MEMS Display

Pixels released using XeF₂.

Image Courtesy of Qualcomm
RF Switch

Side-View Illustration and Photograph of XeF₂ Released Cantilever Switch

Image Courtesy of IBM
Nano-Mechanical Sensors For Virus Detection

- Dr. Rashid Bashir, Purdue University.
- Very small cantilevers for airborne virus detection (30nm X 1.5µm X 4µm)
- Isotropic nature and high selectivity to oxide used to release very small cantilevers of different dimensions in the same process steps.

A. Gupta, D. Akin, R. Bashir, http://www.ece.purdue.edu/~bashir
ZnO Resonators

- Dr. Don DeVoe, University of Maryland
- Used XeF$_2$ to release mixed material resonators including ZnO, Al and SiO$_2$

Deep Trench Etch Stops

- High selectivity allows very thin oxide etch stops.
- Build perfectly rigid and dimensionally precise anchor points.

Bolometer Structures and Thermal Isolation in IR Sensors

- Sensor array for Mitsubishi IR-SC1 camera
- Isotropic etching of silicon to create insulating space beneath the sensor.
- Etching both poly and bulk silicon

Covered Trenches

- Georgia Tech
- Covered Trenches as Part of Sensor Structure
- Created using sacrificial polysilicon and XeF2.

Image Courtesy of Dr. Oliver Brand, Georgia Tech.
PZT Pump

- PZT Membrane Pump
- Released using XeF$_2$ to etch amorphous silicon.
- High selectivity allows very long undercut.

Photo courtesy of The Pennsylvania State University and Northrop Grumman Corporation
Polymer Covered Microchannels

- Carnegie Mellon University MEMS Laboratory
- Etching through porous polymer membrane to make microchannels.

Cooling Tubes Etched At Bottom of DRIE Trench

- Carnegie Mellon University MEMS Laboratory
- Polymer protecting sidewall in Bosch process used as mask for isotropic etch with xenon difluoride.

Nanocapillaries

- Adriatic Research Institute
- Silicon Nitride Nanocapillaries
  - 25nm to 100nm in diameter.
  - Up to 5um long.
- Created using sacrificial silicon and XeF2.

Ultra-high-Q Toroid Microcavities on a Chip

• Dept. of Applied Physics, California Institute of Technology

• A combination of wet-etching and isotropic XeF2-etching is used to create equally undercut circular silica disks on a silicon support pillar.

http://www.its.caltech.edu/~vahalagr/
Self Assembled Micro Toroid

- University of Louisville
- Material stress used to achieve desired shape after release using XeF$_2$ from base material.
Poly-SiC Membrane with Subwavelength Hole Arrays

- Stanford
- Silicon Carbide array with 5um openings released using XeF$_2$
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Failure Analysis

- Gently remove silicon to reveal circuit structures.
- Remove backside silicon while preserving oxide buried layer.
- Stop on gate oxide and trench oxides.
- Etch through extremely small openings and thin layers.
- Use tape, photo-resist, other materials as temporary mask.
- Etch in package without damaging packaging materials.
- Remove Ta, Ti, W, TiN, TaN without damaging layers underneath.
- Remove silicon caps.
Polysilicon Removal

Polysilicon 2 Removed Without Damaging Dielectric Layer Underneath
Back Side Silicon Removal from SOI

Silicon Removed From Backside Of Processor Implemented Using SOI
Back Side Removal of Si from Non SOI

Silicon Removed From Backside of Circuit, Stopping on Gate and Trench Oxide
Metal Etches

- Ta, TaN, Ti, TiN, W, TiW
- Etch rates are known to be temperature sensitive.
- Lower temperatures give lower etch rates
- Ta, TaN used as boundary layers for Cu.
- Ti, TiN used as boundary layers for Al.
- Ti used as adhesion layer for Au.
Example Etching Ti and TiN

- Run on CVE chamber with 10°C to 50 °C chuck temp.
- Ti and TiN in contact with silicon so temperature at etchfront higher due to exothermic Si etch reaction.
- No etching at lower temperatures, etching starts near 50°C chuck temp.
Example Etching Ta and TaN

- Samples on non silicon wafers.
- Temperatures varied between 10°C and 100°C.
- Conclusion: increase in temperature significantly increased etch rate of Ta and TaN.
- Etch rates increased from nearly zero to 30nm/min.
- Inflection point between 60°C and 90°C.
Tungsten

- Tungsten etches more readily than Ti, Ta, TiN and TaN.
- At very low temperatures etching rate can be near zero.
Metal Etch Conclusion

- W etches readily in XeF$_2$
- Ti, Ta, TiN, TaN
  - Little or no etching below 60°C
  - Etch rates > 300Å/min above 90°C
Restore Die Strength After Dicing

- **Problem**
  - After dicing, especially with laser dicing, die lose strength and break during packaging.
  - Problem is worst for die under 75um thick

- **Solution**
  - Short exposure to XeF₂ after dicing
  - Removes Poly-Si after laser dicing.
  - Heals cracks in substrate.
  - Treat etched wafers with no damage to dicing tape or dicing frame.
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Xetch e1 Series™
MEMS Release for Universities

Expands Research Possibilities
Backed by the Market Leader

- Affordable
- Reliable
- Flexible
- Multiuser Control Software
- Low Cost of Ownership
The Xetch® X3B and X3C
*R&D Through Pilot Production*

Leading Xenon Difluoride System for MEMS Release

• Accelerated Etch Rates
• High Repeatability
• Sophisticated Control
• Low Cost of Ownership
The Xetch® X3M
*Volume Production*

**Low Cost Solution for Volume Production**

- Etch wafers as a batch in the wafer boat.
- 4” and 6” capability
- Low Cost of Ownership
The Xetch® XT

Low Cost Solution for Volume Production

• Etch larger substrates

• Etch large batches of smaller substrates
STS XeF$_2$ Module

*Volume Production*

Leading Xenon Difluoride System for MEMS Volume Production

- Module for STS Wafer Handling Platform
- Multiple Wafer Handling Options
- 6” and 8” Capabilities
- Combine with Other STS Tools in Cluster Configuration.
XACTIX Etchers

• Very Reliable and Durable
  – Customers use their Xetch 24 and 7
  – Customers say Xetch is the most reliable piece of equipment in their fab

• Low Cost of Ownership
  – Small power requirements.
  – Common gasses (nitrogen & dry compressed air)
  – Low regular maintenance costs
  – Low training costs

• Very Flexible
  – Wide Variety of Models for R&D and Volume Production
  – Etch wafers, portions of wafers, die or packaged parts
Conclusion

• XeF$_2$ Isotropic Etch: Si, Mo, Ge
• Possible to etch W, TiW, Ti, Ta, TiN and TaN
• Very Low or No Attack on Most Other Materials
• Increased Yield, Improved Device Performance, Improved Processes
• Wide Range of Application Areas and Device Structures
• Wide Range of Equipment Options for R&D and Volume Production
• Combine XeF$_2$ with Other Process Modules on the STS Platform
• Unequaled Experience and R&D Using XeF$_2$: XACTIX and STS